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10/529,503	10/25/2005	Masaki Kitaoka	SUGI-101US	6154
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RATNERPRESTIA P O BOX 980 VALLEY FORGE, PA 19482-0980				MCCOMMAS, STUART S
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,503	KITAOKA ET AL.	
	Examiner	Art Unit	
	Stuart McCommas	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 28 March 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-24 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-24 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____.
 5) Notice of Informal Patent Application
 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang (United States Patent 6,268,840), hereinafter referenced as Huang.

Regarding claim 1, Huang discloses a method for driving a cholesteric liquid crystal display device in which a cholesteric liquid crystal is driven in a matrix manner by means of a plurality of common electrodes (1162) and segment electrodes (1182), the common electrodes and segment electrodes being crossed oppositely (figure 2), the method comprising the steps of:

writing display content to the cholesteric crystal by sequentially applying common electrode drive voltage waveforms from the common electrodes (1162) to the cholesteric liquid crystal display device, the common electrode drive voltage waveforms including a reset voltage waveform to cause the cholesteric liquid crystal to enter a homeotropic state, a select voltage waveform to select a final alignment state of the cholesteric liquid crystal, a hold voltage waveform to hold an alignment state selected by the select voltage waveform, and a non-select voltage waveform caused by a matrix drive (column 5 lines 6-67; column 6 lines 1-4; column 6 lines 26-67; column 7 lines 1-20; figures 3A-3B; figures 4A-4F; figures 6A-6D; figure 7).

applying segment electrode drive voltage waveforms from the segment electrodes (1182) to the cholesteric liquid crystal display device during the step of writing the display content, the segment electrode drive voltage waveforms including at least an ON voltage waveform for determining the final alignment state of the cholesteric liquid crystal as a planar alignment state (figures 6A-6D), and an OFF voltage waveform for determining the final alignment state as a focal conic state (column 5 lines 60-67; column 6 lines 1-4; figures 3A-3B; figures 6A-6D).

wherein the common electrode drive voltage waveforms are formed so that there is no period of time during which the same voltage is applied to all common electrodes at the same time in a period of time from the application of the hold voltage waveform to the first common electrode to the application of the reset voltage waveform to the last common electrodes, during the step of writing a display content when different voltages are applied to the common electrodes during each period (column 10 lines 33-67; column 11 lines 1-6; figures 4A-4F; figures 6A-6D), and the segment electrode drive voltage waveforms are formed so that there is a period of time during which the same voltage is applied to all segment electrodes at the same time during the step of writing the display content when every pixel in the display is off (column 10 lines 16-32; figures 4A-4F; figures 6A-6D).

Regarding claim 2, Huang discloses everything as applied above, further Huang discloses that each of the reset, select, hold, non-select, ON and OFF voltage waveforms has the same number of unit intervals (figures 6A-6D), and each of the reset, select, hold, non-select voltage waveforms has two levels of voltages in the same

unit interval (figures 6A-6D), and each of the ON and OFF voltage waveforms has two or less levels of voltages in the same unit interval (figures 6A-6D).

Regarding claim 3, Huang discloses everything as applied above, further Huang discloses that each of the reset, select, hold, and non-select voltage waveforms has two levels of voltages (figures 6A-6D).

Regarding claim 4, Huang discloses everything as applied above, further Huang discloses that each of the reset, select, hold, and non-select voltage waveforms has three levels of voltages (figures 6A-6D).

Regarding claim 5, Huang discloses everything as applied above, further Huang discloses that each of the reset, select, hold, and non-select voltage waveforms has four levels of voltages (figures 6A-6D).

Regarding claim 6, Huang discloses everything as applied above, further Huang discloses that the maximum voltage value of the reset voltage waveform and the maximum voltage value of the hold voltage waveform are the same voltage value of 60 volts (figures 6A-6D).

Regarding claim 7, Huang discloses everything as applied above, further Huang discloses that each of the ON and OFF voltage waveforms has three or four levels of voltages (figures 6A-6D).

Regarding claim 8, Huang discloses everything as applied above, further Huang discloses that each of the ON and OFF voltage waveforms has two levels of voltages (figures 6A-6D).

Regarding claim 9, Huang discloses everything as applied above, further Huang

discloses that the ON and OFF voltage waveforms and the non-select voltage waveform applied to the columns are the same (figures 6A-6D).

Regarding claim 10, Huang discloses everything as applied above, further Huang discloses that the select and non-select voltage waveforms are the same (figures 6A-6D).

Regarding claim 11, Huang discloses a cholesteric liquid crystal display apparatus comprising:

a liquid crystal display device in which a plurality of picture elements are formed at portions crossed by a plurality of common electrodes (1162) and segment electrodes (column 4 lines 44-50; figure 2; figure 7);

a common driver (row driver 150) for writing display content to the picture elements by sequentially applying drive voltage waveforms from the common electrodes to the cholesteric liquid crystal display device (column 11 lines 8-50; figure 7), the drive voltage waveforms including a reset voltage waveform to cause the cholesteric liquid crystal to enter a homeotropic state, a select voltage waveform to select a final alignment state of the cholesteric liquid crystal, a hold voltage waveform to hold an alignment state selected by the select voltage waveform, and a non-select voltage waveform caused by a matrix drive (column 5 lines 6-67; column 6 lines 1-4; column 6 lines 26-67; column 7 lines 1-20; figures 3A-3B; figures 4A-4F; figures 6A-6D; figure 7);

a segment driver (column driver 200) for applying drive voltage waveforms from the segment electrodes to the cholesteric liquid crystal display device during the step of writing a-the display content, the drive voltage waveforms including at least an ON

voltage waveform for determining the final alignment state of the cholesteric liquid crystal as a planar alignment state, and an OFF voltage waveform for determining the final alignment state as a focal conic state (column 5 lines 60-67; column 6 lines 1-4; column 11 lines 51-64; figures 3A-3B; figures 6A-6D; figure 7);

a controller (250) for controlling the common driver and segment driver (column 12 lines 3-19; figure 7);

wherein the controller controls the common and segment driver in such a way that each of the reset, select, hold, non-select, ON and OFF voltage waveforms has the same number of unit intervals, each of the reset, select, hold, non-select voltage waveforms has two levels of voltages in the same unit interval, and each of the ON and OFF voltage waveforms has two or less levels of voltages in the same unit interval (figures 6A-6D).

Regarding claim 12, Huang discloses everything as applied above, further Huang discloses that the controller (250) controls the common driver in such a way that there is no period of time during which the same voltage is applied to all common electrodes in a period of time from the application of the hold voltage waveform to the first common electrode to the application of the reset voltage waveform to the last common electrodes during a step of writing a-the display content (column 10 lines 33-67; column 11 lines 1-6; figures 4A-4F; figures 6A-6D), and that there is a period of time during which the same voltage is applied to all segment electrodes during the step of writing the display content (column 10 lines 16-32; figures 4A-4F; figures 6A-6D).

Regarding claim 13, Huang discloses everything as applied above, further Huang discloses that the controller (250) controls the common driver in such a way that the voltages applied to the common electrodes have two levels of voltages (figures 6A-6D).

Regarding claim 14, Huang discloses everything as applied above, further Huang discloses that the controller controls the common driver in such a way that the voltages applied to the common electrodes have three levels of voltages V_h , V_m , and V_1 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the common electrodes include V_h and V_m (figures 6C-6D) and a unit interval during which the voltages applied to the common electrodes include V_m and V_1 (figures 6A-6B).

Regarding claim 15, Huang discloses everything as applied above, further Huang discloses that the controller controls the common driver in such a way that the voltages applied to the common electrodes have three levels of voltages V_h , V_m , and V_1 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the common electrodes include V_h and V_1 (figures 6A-6D) and a unit interval during which the voltages applied to the common electrodes include V_m and V_1 (figures 6A-6B).

Regarding claim 16, Huang discloses everything as applied above, further Huang discloses that the controller controls the common driver in such a way that the voltages applied to the common electrodes have three levels of voltages V_h , V_{mh} , V_{ml} , and V_1 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the common electrodes include V_h and V_1 (figures 6A-6D), and

a unit interval during which the voltages applied to the common electrodes include V_m and V_1 (figures 6A-6B), and a unit interval during which the voltages applied to the common electrodes include V_{mh} and V_{ml} (figures 6B-6C).

Regarding claim 17, Huang discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have four levels of voltages V_1 , V_2 , V_3 and V_4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V_1 (figure 17), and a unit interval during which the voltages applied to the segment electrodes include V_1 and V_2 (figures 17-22), and a unit interval during which the voltages applied to the segment electrodes include V_3 and V_4 (figures 17-22).

Regarding claim 18, Huang discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have three levels of voltages V_1 , V_2 , and V_4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V_1 (figures 6A-6D; figures 17-22), and a unit interval during which the voltages applied to the segment electrodes include V_2 and V_4 (figures 17-22).

Regarding claim 19, Huang discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have three levels of voltages V_1 , V_2 , and V_4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during

which the voltages applied to the segment electrodes include V4 (figures 6A-6D; figures 17-22), and a unit interval during which the voltages applied to the segment electrodes include V1 and V2 (figures 17-22).

Regarding claim 20, Huang discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have three levels of voltages V1, V2, and V4 (figures 6A-6D; figures 17-22), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V2 (figures 6A-6D; figures 17-22), a unit interval during which the voltages applied to the segment electrodes include V4 (figures 6A-6D; figures 18-22), and a unit interval during which the voltages applied to the segment electrodes include V1 and V2 (figures 6A-6D; figures 17-22).

Regarding claim 21, Huang discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have three levels of voltages V1, V2, and V4 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V1 (figures 6A-6D), a unit interval during which the voltages applied to the segment electrodes include V2 (figures 6A-6D), a unit interval during which the voltages applied to the segment electrodes include V4 (figures 6A-6D), and a unit interval during which the voltages applied to the segment electrodes include V2 and V4 (figures 6A-6D; figures 17-22).

Regarding claim 22, Huang discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages

applied to the segment electrodes have four levels of voltages V1, V2, and V4 (figures 6A-6D), and include, for writing a display content, a unit interval during which the voltages applied to the segment electrodes include V1 (figures 6A-6D), a unit interval during which the voltages applied to the segment electrodes include V4 (figures 6A-6D), and a unit interval during which the voltages applied to the segment electrodes include V2 and V4 (figures 6A-6D; figures 17-22).

Regarding claim 23, Huang discloses everything as applied above, further Huang discloses that the controller controls the segment driver in such a way that the voltages applied to the segment electrodes have two levels of voltages (figures 6A-6D; figures 17-22).

Regarding claim 24, Huang discloses everything as applied above, further Huang discloses that the controller controls the common and segment drivers in such a way that the voltages applied to the common and segment electrodes are 42 volts or less (figures 6A-6D).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart McCommas whose telephone number is (571)270-3568. The examiner can normally be reached on Monday-Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on (571)272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stuart McCommas
Patent Examiner
Art Unit 2629

SSM

/Alexander Eisen/
Supervisory Patent Examiner, Art Unit 2629